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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,499	03/24/2004	David John Butcher	550-540	4256

23117 7590 10/05/2006

NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,499	BUTCHER ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004 and 21 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/24/04; 9/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-48 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Abstract, Specification, Claims, and Drawings as received on 24 March 2004; Authorization for Extension of Time All Replies as received on 24 March 2004; IDS as received on 24 March 2004; Abstract, Specification, Claims, Drawings, and Oath and Declaration as received on 27 July 2004; and IDS as received on 21 September 2005.

Information Disclosure Statement

3. The information disclosure statement filed 24 March 2004, with regards to C. Glossner et al, "Parallel Processing" Euro-Pan 1997 (Passau, Germany, 8/1997) and M. Ibrahinn et al., "Signal Processing Systems *(SIPS 97) Design and Implementation*", 1997 IEEE Workshop, 11/1997, fail to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered. The item is merely a table of contents for the papers presented at the conference and the relevance of this table of contents has not been explained. None of the papers have been specifically identified or provided and the relevance of this citation is unclear.

4. The citation of "Y. Patt et al. *Introduction to Computing Systems from Bits and Gates to C and Beyond*, 2001, pages 1-16, 91-118, & 195-209" was marked through, since it was a duplicate listing. These cited pages were considered when the citation "Y. Patt et al.

Introduction to Computing Systems from Bits and Gates to C and Beyond, 2001, pages 1-526" was considered.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 25-48 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. These claims are for computer program products, including a computer program, which is non-statutory subject matter. A computer program is not patentable subject matter.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-5, 7, 9-11, 13-17, 19, 21-23, 25-29, 31, 33-35, 37-41, 43, and 45-47 are rejected under 35 U.S.C. 102(b) as being taught by Ishizaki et al., U.S. Patent Number 6,484,314 (herein referred to as Ishizaki).

9. Referring to claims 1, 13, 25, and 37, taking claim 1 as exemplary, Ishizaki has taught apparatus for processing data comprising:

a. Processing logic operable to perform data processing operations (Ishizaki column 6, lines 11-29; Figure 4; and Figure 5). In regards to Ishizaki, the processing logic

is inherent to the CPU of Ishizaki. See FOLDOC "central processing unit" ©1998 and "arithmetic and logic unit" ©1995 for more information.

b. An instruction decoder operable to decode program instructions to control said processing logic to perform data processing operations specified by said program instructions (Ishizaki column 6, lines 11-29; Figure 4; and Figure 5). In regards to Ishizaki, the processing logic is inherent to the CPU of Ishizaki. See FOLDOC "central processing unit" ©1998, "control unit" ©1995, and "machine cycle" ©1995 for more information.

c. Wherein said instruction decoder is responsive to a compare and branch instruction (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; and column 2, lines 4-11):

i. To perform a comparison between a first value stored in a first register and a second value stored in a second register (Ishizaki column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10);

ii. To determine a target branch address from a pre-programmed stored value (Ishizaki column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10); and

iii. To branch to a sub-routine at said target branch address in dependence upon a result of said comparison (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; column 2, lines 4-11; column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10).

10. Claims 13, 25, and 37 contain similar limitations to claim 1 and are rejected for similar reasons. The claims differ from claim 1 in that claim 13 is a method and claims 25 and 37 are computer program products.

11. Regarding to claims 2, 14, 26, and 38, Ishizaki has taught, taking claim 2 as exemplary, apparatus as claimed in claim 1, wherein said instruction is an array bounds checking instruction and said sub-routine is an array bounds exception handling routine (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; column 2, lines 4-11; column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10). Claims 14, 26, and 38 contain similar limitations to claim 2 and are rejected for similar reasons.

12. Regarding claims 3, 15, 27, and 38, Ishizaki has taught, taking claim 3 as exemplary, apparatus as claimed in claim 1, wherein at least one of said first register and said second register are specified within said compare and branch instruction (Ishizaki column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10). Claims 15, 27, and 38 contain similar limitations to claim 3 and are rejected for similar reasons.

13. Regarding claims 4, 16, 28, and 40, Ishizaki has taught, taking claim 4 as exemplary, apparatus as claimed in claim 2, wherein said first value is a reference value specifying an array size and said second value is a test value determined from a decoded program instruction (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; column 2, lines 4-11; column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10). Claims 16, 28, and 40 contain similar limitations to claim 4 and are rejected for similar reasons.

14. Regarding claims 5, 17, 29, and 41, Ishizaki has taught, taking claim 5 as exemplary, apparatus as claimed in claim 4, wherein said comparison determines whether said reference

value is greater than or equal to said test value (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; column 2, lines 4-11; column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10). Claims 17, 29, and 41 contain similar limitations to claim 5 and are rejected for similar reasons.

15. Regarding claims 7, 19, 31, and 43, Ishizaki has taught, taking claim 7 as exemplary, apparatus as claimed in claim 2, wherein said branching operation comprises copying a pointer to said array bounds exception handling routine into a register specifying a next program instruction (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; and column 2, lines 4-11). Claims 19, 31, and 43 contain similar limitations to claim 7 and are rejected for similar reasons.

16. Regarding claims 9, 21, 33, and 45, Ishizaki has taught, taking claim 9 as exemplary, apparatus as claimed in claim 1, wherein said compare and branch instruction is executed within a single processing cycle of said data processing apparatus when the branch is not taken (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; column 2, lines 4-11; column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10). Claims 21, 33, and 48 contain similar limitations to claim 9 and are rejected for similar reasons.

17. Regarding claims 10, 22, 34, and 46, Ishizaki has taught, taking claim 10 as exemplary, apparatus as claimed in claim 1, wherein said instruction decoder is operable to decode translated platform-independent program instructions (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; and column 2, lines 4-11). Claims 22, 34, and 46 contain similar limitations to claim 10 and are rejected for similar reasons.

18. Regarding claims 11, 23, 35, and 47, Ishizaki has taught, taking claim 11 as exemplary, apparatus as claimed in claim 10, wherein said platform independent program instructions are one of:

a. Java bytecodes (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; and column 2, lines 4-11);

b. .net bytecodes;

c. MSIL bytecodes; and

d. CIL bytecodes.

19. Claims 22, 34, and 46 contain similar limitations to claim 10 and are rejected for similar reasons.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 6, 18, 30, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizaki et al., U.S. Patent Number 6,484,314 (herein referred to as Ishizaki), as applied to claims 4, 16, 28, and 40 above, in view of "The Art of Assembly Programming" ©30 September 1996 (herein referred to as Assembly Programming). Taking claim 6 as exemplary, Ishizaki has not taught apparatus as claimed in claim 4, wherein said result of said comparison is determined from a carry flag value and zero flag value. Assembly Programming has taught wherein said result of said comparison is determined from a carry flag value and zero flag value (Assembly

Programming Sections 6.5.3 and 6.9.4). Ishizaki has taught in column 5, line 17 that a greater than or equal to compare and branching instruction is performed. However, Ishizaki has not taught explicitly how the compare functions, e.g. how the results are determined, and how the compare instruction directly affects the jump function. Assembly Programming has explicitly taught a method for the compare instruction, which only sets the flags register (Assembly Programming Section 6.5.3), and that the compare instruction flag results directly influence the conditional jumps (Assembly Programming Section 6.9.4). A person of ordinary skill in the art at the time the invention was made would have recognized that the compare and jumps of Assembly Programming implements the compare and jumps without using too much memory, since it does not need to store the subtraction results. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the compare and jumps of Assembly Programming in the device of Ishizaki. Claims 18, 30, and 42 contain similar limitations to claim 6 and are rejected for similar reasons.

22. Claims 8, 20, 32, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizaki et al., U.S. Patent Number 6,484,314 (herein referred to as Ishizaki), as applied to claims 1, 13, 25, and 37 above, in view of Schmidt et al., U.S. Patent Number 5,727,227 (herein referred to as Schmidt). Taking claim 8 as exemplary, Ishizaki has not explicitly taught apparatus as claimed in claim 1, wherein said data processing apparatus comprises a co-processor and said pre-programmed stored value is read from a register of said co-processor. Schmidt has taught wherein said data processing apparatus comprises a co-processor and said pre-programmed stored value is read from a register of said co-processor (Schmidt column 3, line 45 to column 4, line 49; Figure 1; and Figure 3). Ishizaki has taught in column 6, lines 28-29 that a multi-CPU

configuration may be used, but has not taught the specific functions of each CPU or their purpose in the system. Schmidt has explicitly taught the functions of each CPU in a multi-CPU system and their purpose in the overall system. A person of ordinary skill in the art at the time the invention was made, and as taught by Schmidt, would have recognized that the co-processor system of Schmidt reduces the amount of time needed to process interrupt/exception routines, thereby improving the speed of the system (Schmidt column 3, lines 33-43). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the co-processor of Schmidt in the device of Ishizaki to improve processor speed. Claims 20, 32, and 44 contain similar limitations to claim 8 and are rejected for similar reasons.

23. Claims 12, 24, 36, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizaki et al., U.S. Patent Number 6,484,314 (herein referred to as Ishizaki), as applied to claims 1, 13, 25, and 37 above, in view of Wikipedia term "Protected Mode" ©October 2003 (herein referred to as Wikipedia). Taking claim 9 as exemplary, Ishizaki has taught an apparatus as claimed in claim 1, said data processing apparatus remains in a user mode during execution of said compare and branch instruction (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; column 2, lines 4-11; column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10). Ishizaki has not taught wherein said data processing apparatus is operable in a user mode and a privileged mode. Wikipedia has taught wherein said data processing apparatus is operable in a user mode and a privileged mode (Wikipedia term "Protected mode"). A person of ordinary skill in the art at the time the invention was made would have recognized that protected mode does not allow other tasks to see the current tasks memory, thereby making multi-tasking more stable (Wikipedia term "Protected mode"). Therefore, it would have been obvious to a

person of ordinary skill in the art at the time the invention was made to incorporate the modes of Wikipedia in the device of Ishizaki to make the system more stable for multi-tasking. Claims 24, 36, and 48 contain similar limitations to claim 12 and are rejected for similar reasons.

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Rodgers et al., U.S. Patent Number 5,889,982, has taught event handlers with conditional branching to the software handlers.

b. Tremblay et al., U.S. Patent Number 6,014,723, has taught array boundary checking with compares.

c. Dijkstra, U.S. Patent Number 6,789,098, has taught compare and branches.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
28 September 2006

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100